**IN THE CLAIMS:**

Please amend the claims as follows (all claims listed):

Claims 1.-20. (Cancelled)

21. (Currently Amended) A method of pausing processing of instructions, comprising:

determining whether a first instruction for a first thread is an instruction of a first type at a pipeline stage of a processor;

pausing processing of instructions of said first thread at said pipeline stage for a period of time if said first instruction is of a first type while processing instructions from a second thread at said pipeline stage; and

resuming processing of ~~instruction~~ instructions of said first thread responsive to the determining operation ~~said first instruction~~ at said pipeline stage.

22. (Currently Amended) The method of claim [[~~34~~]] 21 further comprising decoding said first instruction into a first microinstruction and a second microinstruction.

23. (Currently Amended) The method of claim [[~~35~~]] 22 wherein said first microinstruction causes a value to be stored in memory for said first thread.

24. (Currently Amended) The method of claim [[~~36~~]] 23 further comprising:

processing said second microinstruction for execution when said value stored in memory is reset.

25. (Currently Amended) The method of claim [[~~37~~]] 24 wherein said value stored in memory is reset ~~when~~ if said first microinstruction is retired.

26. (Currently Amended) A method comprising:

determining whether a first instruction of a first thread is an instruction of a first type;

initiating a counter; and

pausing processing of instructions of said first thread at a pipeline stage of a processor until said counter reaches a predetermined value while processing instructions for a second thread at said pipeline stage.

27. (Currently Amended) The method of claim [[~~39~~]] 26 wherein said first instruction includes an operand and said initiating includes loading said counter with said operand.

28. (Currently Amended) The method of claim [[~~40~~]] 27 further comprising resuming processing instructions of said first thread after said counter reaches said predetermined value.

29. (Currently Amended) An apparatus, comprising:

a decode unit to determine whether a first instruction of a first thread is an instruction of a first type, said decode unit to pause processing of instructions of said first thread at a pipeline stage of a processor for a period of time while instructions from a second thread can be processed, said decode unit further to cause resumption of processing instructions of said first thread in response to the determination at said decode unit ~~said first instruction~~.

30. (Currently Amended) The apparatus of claim [[~~42~~]] 29 wherein said first instruction comprises a first microinstruction and a second microinstruction.

31. (Currently Amended) The apparatus of claim [[~~43~~]] 30 further comprising:

a memory, wherein the determination at said decode unit is to cause ~~said first~~

~~microinstruction causes~~ a value to be stored in memory for said first thread.

32. (Currently Amended) The apparatus of claim [[~~44~~]] 31 wherein said decode unit ~~processes~~ is to process said second microinstruction ~~when~~ if said value stored in memory is reset.

33. (Currently Amended) The apparatus of claim [[~~45~~]] 32 further comprising:

a retire unit coupled to said decode unit wherein said retire unit ~~causes~~ is to cause said value stored in memory to be reset ~~when~~ if said first microinstruction is retired by said retire unit.

34. (Currently Amended) An apparatus comprising:

a decode unit to determine whether a first instruction for a first thread is an instruction of a first type;

a counter coupled to said decode unit, said counter to be initiated if said first instruction for said first thread is an instruction of said first type, said decode unit to pause processing instructions of said first thread at a pipeline stage of a processor until said counter reaches a predetermined value; and

wherein instructions for a second thread can be processed while instructions of said first thread are paused from being processed and wherein said decode unit ~~resumes~~ is to resume processing instructions of said first thread in response to the determination at said decode unit ~~said first instruction~~.

35. (Currently Amended) The apparatus of claim [[~~47~~]] 34 wherein said first instruction includes an operand to be loaded into said counter.

36. (Currently Amended) The apparatus of claim [[~~48~~]] 35 wherein said decode unit can continue to operate while said first thread is paused from being processed.